

SPICE Device Model Si4947ADY

Vishay Siliconix

Dual P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

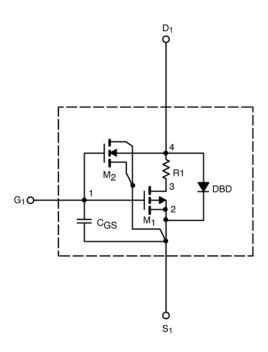
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

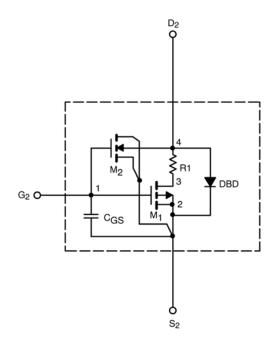
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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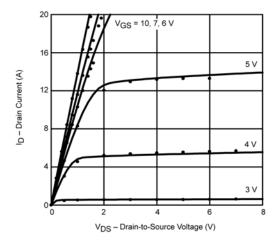
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	•				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	2.2		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	62		Α
Drain-Source On-State Resistance ^a	r _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -3.9 \text{ A}$	0.071	0.062	Ω
		V _{GS} = -4.5 V, I _D = -3. A	0.12	0.105	
Forward Transconductance ^a	g _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -2.5 \text{ A}$	5	5	S
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = -1.7 A, $V_{\rm GS}$ = 0 V	-0.80	-0.82	V
Dynamic ^b					
Total Gate Charge	Q _g	$V_{DS} = -10 \text{ V}, V_{GS} = -5 \text{ V}, I_D = -3.9 \text{ A}$	5.3	5.8	nC
Gate-Source Charge	Q_{gs}		2	2	
Gate-Drain Charge	Q_{gd}		1.9	1.9	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$	11	8	ns
Rise Time	t _r		7	9	
Turn-Off Delay Time	t _{d(off)}		21	21	
Fall Time	t _f		6	10	

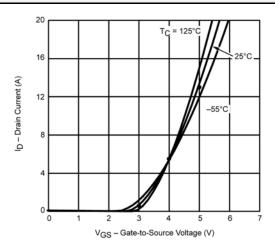
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

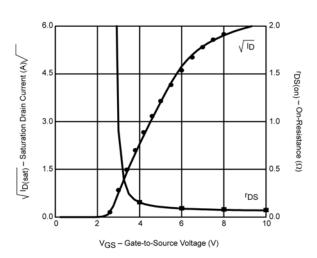


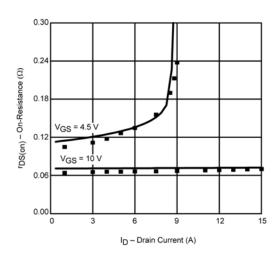
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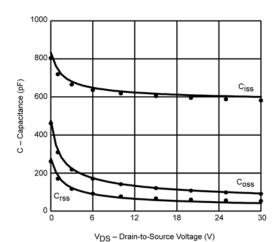
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

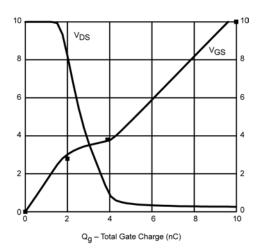












Note: Dots and squares represent measured data.



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